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CERTIFICATE OF TRANSMISSION**November 9, 2004**

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|--------------------------|----------------|
| Atty Docket No. : | JCLA4020 |
| Appl. No. : | 09/895,559 |
| Filing Date : | June, 28, 2001 |
| Pages : | Cover + 13 |

BY FACSIMILE ONLY

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|---------------------|--|
| Fax No. : | 703-872-9306 |
| Attention : | EXAMINER : ABRAHAM, ESAW T. |
| Group Unit : | 2133 |
| From : | Jiawei Huang, Reg. No. 43,330 |
| MESSAGE : | Enclosed herewith is an Amendment with amended drawings in 13 pages. |

Sir:

I hereby certify that this correspondence is being facsimile transmitted to the Patent and Trademark Office on **November 9, 2004** at the above indicated fax number.

Sign by


Michelle Chang

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Application No.: 09/895,559

NOV 09 2004

Docket No.: JCLA4020

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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|----------------------------------|---|-----------------------------|
| In Re Application of : |) | |
| |) | |
| Hsiao <i>et al.</i> |) | Examiner : Abraham, Esaw T. |
| |) | |
| Serial No.: 09/895,559 |) | Art Unit : 2133 |
| |) | |
| Filed : 06/28/2001 |) | Docket No.: JCLA4020 |
| |) | |
| For : Testing Architecture for a |) | |
| Semiconductor Memory Device |) | |

No fee is believed to be due. However, the Commissioner is authorized to charge any fees required in connection with the filing of this paper to account No. 50-0710 (Order No. JCLA4020).

AMENDMENT AND RESPONSE TO OFFICE ACTION

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In reply to the Office Action dated August 12, 2004, Applicants respectfully submit the following Amendments and Remarks.

Page 1 of 11

Application No.: 09/895,559

Docket No.: JCLA4020

AMENDMENTS

Please amend the application as indicated hereafter.

In the Title:

Please amend the title as follows:

TESTING ~~ARCHITECTURE FOR A~~ SYSTEM FOR SEMICONDUCTOR MEMORY
DEVICE.

In the Specification:

Please amend the paragraphs as follows.

Paragraph beginning at page 2, line 6:

Before the tester ~~130-10~~ starts testing, a stop signal is transmitted to the DUT 130 through line 132 to stop transmitting data to the SIPO 110. This is called a hardware time delay. The time delay can benefit the testing process. An access signal output from the tester 130 is transmitted to the buffer 120 through line 134. The 8 bits of data stored in the buffer 120 is transmitted to the tester 130 through bus 122.